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APPLICATION FOR UNITED STATES LETTERS PATENT

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STRAINED finFETs AND METHOD OF MANUFACTURE

DESCRIPTION

BACKGROUND OF THE INVENTION

Field of the Invention

The invention generally relates to a semiconductor device and method of manufacture and, more particularly, to the fabrication of finFETs of a semiconductor device with tensile and compressive stresses.

Background Description

Mechanical stresses within a semiconductor device substrate can modulate device performance. That is, stresses within a semiconductor device are known to enhance semiconductor device characteristics. Thus, to improve the characteristics of a semiconductor device, tensile and/or compressive stresses are created in the channel of the n-type devices (e.g., nFETs) and/or p-type devices (e.g., pFETs). However, the same stress component, either tensile stress or compressive stress, discriminatively affects the characteristics of an n-type device and a p-type device.

In order to maximize the performance of both nFETs and pFETs within integrated circuit (IC) chips, the stress components should be engineered and applied differently for nFETs and pFETs. That is, because the type of stress which is beneficial for the

performance of an nFET is generally disadvantageous for the performance of the pFET. More particularly, when a device is in tension (e.g., in the direction of current flow in a planar device), the performance characteristics of the nFET are enhanced while the performance characteristics of the pFET are diminished. To selectively create tensile stress in an nFET and compressive stress in a pFET, distinctive processes and different combinations of materials are used.

For example, a trench isolation structure has been proposed for forming the appropriate stresses in the nFETs and pFETs, respectively. When this method is used, the isolation region for the nFET device contains a first isolation material which applies a first type of mechanical stress on the nFET device in a longitudinal direction (e.g., parallel to the direction of current flow) and in a transverse direction (e.g., perpendicular to the direction of current flow). Further, a first isolation region and a second isolation region are provided for the pFET and each of the isolation regions of the pFET device applies a unique mechanical stress on the pFET device in the transverse and longitudinal directions.

Alternatively, liners on gate sidewalls have been proposed to selectively induce the appropriate stresses in the channels of the FET devices (see, Ootsuka et al., IEDM 2000, p.575, for example). By providing liners, the appropriate stress is applied closer to the device than the stress applied as a result of the trench isolation fill technique.

Also, there have been many proposals to improve both nFET and pFET device performance using tensile and compressive stresses, respectively, which include modulating spacer intrinsic stresses and STI (shallow trench isolation) material changes individually for two MOSFETs using masks. Tensilely strained Si on relaxed SiGe has also been proposed as a means to apply this stress. Unfortunately, the tensilely strained Si on relaxed SiGe can apply only biaxial tensile stress on the Si cap as used in stack form. This constrains the regime of Ge% that is useful because of the nature of pFET sensitivity to stress. The nFET performance monotonically improves with biaxial tension; however, the pFET is degraded with biaxial tension until about 3 GPa at which point it begins to improve.

In order to improve both the pFET and nFET simultaneously, the Ge% needs to be high, approximately greater than 25-30% (or equivalent to approximately greater than 3-4 GPa in stress). This level of Ge% is difficult to implement into processes and is not very manufacturable with major issues including surface roughness, process complexity, defect and yield control, to name but a few. Given that a high Ge% is hard to use for the pFET (since it would be detrimental because of the relatively low levels of tension), other methods must be devised to improve the device performance.

Additionally, Si:C is know to grow epitaxially on Si where it is inherently tensile. A 1% C content in the Si:C/Si material stack can cause tensile stress levels in the Si:C on the order of 500 MPa. In comparison, in the SiGe/Si system about 6% is needed to cause a 500 MPa compression. This 1% level of C can be incorporated into Si during epitaxial

growth as shown in Ernst et al., VLSI Symp., 2002, p. 92. In Ernst, the Si/Si:C/Si is in a layered channel for nFETs. However, the Si:C part of the structure is not relaxed. Instead, in Ernst, an unrelaxed Si:C is used as part of the channel, itself, with a very thin Si cap. The problem with this approach is that the mobility is not enhanced, but retarded, depending on the C content, from scattering.

While these methods do provide structures that have tensile stresses being applied to the nFET device and compressive stresses being applied along the longitudinal direction of the pFET device, they may require additional materials and/or more complex processing, and thus, resulting in higher cost. Further, the level of stress that can be applied in these situations is typically moderate (i.e., on the order of 100s of MPa). Thus, it is desired to provide more cost-effective and simplified methods for creating large tensile and compressive stresses in the channels nFETs and pFETs, respectively.

SUMMARY OF THE INVENTION

In a first aspect of the invention, a method of manufacturing a structure includes forming a first island of material having a first lattice constant and a second island of material having a second lattice constant. A mask is provided over the first island and the second island to prevent future buckling when sidewalls are grown on the fins. The mask is in tensile stress. A first finFET and a second finFET are formed from the first island and the second island and the mask.

In another aspect, a method of manufacturing a structure includes forming shallow trench isolation (STI) in a substrate with a first material and forming a first island associated with a pFET region and a second material forming a second island associated with an nFET region. A hard mask under tension is formed over the pFET region and the nFET region, which is used to form pFET fin and an nFET fin with a capping layer of the hard mask in the pFET region and the nFET region, respectively. Epitaxial silicon sidewalls are grown on the pFET fin and the nFET fin, where the capping layer prevents buckling of the nFET fin during the formation of the sidewall.

In another aspect of the invention, a semiconductor structure includes a substrate and a relaxed shallow trench isolation (STI) in the substrate. A first finFET comprised of a first material having a first lattice constant and a cap of highly tensile material is provided. A second finFET comprised of a second material having a second lattice constant and a cap of highly tensile material is also provided. A Si epitaxially grown sidewall is provided on the first finFET and the second finFET. The cap of highly tensile material on the second finFET prevents lateral buckling of the second finFET when the Si epitaxial sidewall is grown.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1 through 6 represent a fabrication process to form an intermediate structure in accordance with the invention;

Figures 7 through 10 represent a fabrication process to form an intermediate structure in accordance with another aspect of the invention; and

Figures 11-13 show fabrication processes to form an intermediate structure of the invention using either of the structures of Figure 6 or Figure 10, as a base, in accordance with the invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

This invention is directed to a semiconductor device and method of manufacture which provides desired stresses associated with the nFET and the pFET of CMOS devices for improved device performance. In one approach, SiGe and Si:C islands are obtained in the respective nFET and pFET channels prior to the formation of finFETs. Thereafter a tensile film is formed on the islands. This tensile film, e.g., hard mask, provides a significant amount of lateral stiffness and holds the Si:C fin in place. That is, the tensile hard mask prevents the fin, which is under a highly compressive stress, from buckling, laterally, due in part to asymmetries in the fin expected to form during processing. An epitaxial Si layer is then formed on both relaxed nFET and pFET fins to provide the desired stress conditions of the nFET and the pFET.

A finFET is a double-gate structure, where the silicon body has been turned on its side to form a "fin" of silicon standing perpendicular to the wafer plane. The gate electrode is formed on both sides of the fin, allowing simultaneous definition of both

gates with a single mask level and etch. The fin, as implemented in the invention, is preferably symmetrical with a double gate, but may be asymmetrical with a single gate. It should further be recognized that the finFET provides higher drive-current density without requiring gate oxide thickness reduction and its associated leakage by simply adjusting the dimensions of the fins. In the invention, the finFETs are obtained in a relative stress state, which improves the performance of the device.

Prior to the invention, placement of at least two crystal islands for the fabrication of nFETs and pFETs with different relaxed crystal lattice (different dimensions between the atoms) was only feasible by wafer bonding techniques where the islands have a relatively large size; however, in the invention, the methods yield a unique substrate with small crystal islands which have a relaxed but different crystal structure. In one implementation, the use of high temperature stable amorphous material, e.g., SiO_2, between the islands and the crystal on insulator structure is provided. The unique structure with different (crystal) islands allows for the placement of differently strained layers of optionally different crystals. In a first aspect, the differently strained layers are a tensile SiGe layer or a compressive Si:C layer used to from the finFETs of the invention.

The invention has a seminal and important contribution to the art of making substrates with islands on insulator with multiple crystal lattice constants. In the invention, for example, a first finFET (crystal 1) has a lattice constant $a \geq$ aSi and the second finFET (crystal 2) has a lattice constant $a \leq$ aSi. In one aspect of the invention, as discussed in greater detail below, a Si epitaxial sidewall layer of the invention can be

selectively grown, which will strain tensilely and compressively on the SiGe finFET and Si:C finFeT, respectively.

Referring now to Figure 1, a silicon wafer is shown. Such wafers are commercially available starting substrates for various discrete and integrated circuit (IC) semiconductor device applications. In one implementation, silicon on glass (SOI) wafer may be fabricated using the SIMOX (Separation by IMplanted OXygen) process, which employs high dose ion implantation of oxygen and high temperature annealing to form a BOX (buried oxide) layer in a bulk wafer. As another example, the wafer can be fabricated by bonding a device quality silicon wafer to another silicon wafer (the substrate layer) that has an oxide layer on its surface. The pair is then split apart, using a process that leaves a thin (relative to the thickness of the starting wafer), device-quality layer of single crystal silicon on top of the oxide layer (which has now become the BOX) on the substrate layer. The SOI wafer may also be formed using other processes.

Still referring to Figure 1, an Si layer 20 is formed and patterned to form shallow trench isolation (STI) 25 using standard techniques of pad oxidation, pad nitride deposition, lithography based patterning, reactive ion etching (RIE) of the stack consisting of nitride, oxide, and silicon down to the buried oxide, edge oxidation, liner deposition, fill deposition, and chemical mechanical polish. The STI formation process is well known in the art. In one implementation, high temperature stable amorphous material, e.g., SiO_2, is used for the STI.

Referring to Figure 2, an epitaxial Ge material (layer) 30 is deposited over the surface of the structure using conventional techniques such as chemical vapor deposition methods. For example, ultrahigh vacuum chemical vapor deposition (UHVCVD) may be used in a conventional manner to deposit the Ge layer 30. Other conventional techniques include rapid thermal chemical vapor deposition (RTCVD), limited reaction processing CVD (LRPCVD) and molecular beam epitaxy (MBE). In one embodiment, the thickness of the Ge material may range from 5 to 50 nanometers, or other dimension depending on the thickness of the underlying Si layer which may, for example, range from 30 to 100 nanometers.

An nFET hard mask 35 is provided on a portion of the Ge layer 30 (e.g., at locations of a yet to be formed nFET device). The nFET hard mask 35 may be a nitride hard mask formed using a conventional deposition process such as spin-on coating, CVD, plasma-assisted CVD, ultrahigh vacuum chemical vapor deposition (UHVCVD), rapid thermal chemical vapor deposition (RTCVD), limited reaction processing CVD (LRPCVD) and other like deposition processes.

In Figure 3, the exposed Ge layer 30 is etched and the nFET mask 35 is stripped using techniques known in the art. For example, the Ge layer 30 may be selectively etched using RIE, wet or dry etching.

As shown in Figure 4, a Si:C material 40 (or optionally C) is deposited on the structure, including over the epitaxially deposited Ge material 35. For example, ultrahigh vacuum chemical vapor deposition (UHVCVD) may be used in a conventional manner to

deposit the Si:C (or optionally C) material 40. Other conventional techniques include rapid thermal chemical vapor deposition (RTCVD), limited reaction processing CVD (LRPCVD) and other like processes. In one embodiment, the thickness of the Si:C or C material may range from 5 to 50 nanometers, or other dimension depending on the thickness of the underlying Si layer which may, for example, range from 30 to 100 nanometers. In another aspect, when using C, the thickness may range from 1 to 30 nanometers.

A pFET hard mask 45 is provided on a portion of the Si:C material 40 at locations of the yet to be formed pFET. The pFET hard mask 45 may be a nitride hard mask formed using a conventional deposition process such as spin-on coating, CVD, plasma-assisted CVD, ultrahigh vacuum chemical vapor deposition (UHVCVD), rapid thermal chemical vapor deposition (RTCVD), limited reaction processing CVD (LRPCVD) and other like deposition processes.

As shown in Figure 5, the exposed Si:C layer 40 is then etched and the pFET mask 45 is stripped using techniques known in the art. For example, the Si:C and pFET may be etched using standard etching techniques such as, for example, RIE, wet or dry etching and the like.

In Figure 6, the structure then undergoes a thermal annealing process. During this process, for the nFET device, the deposited Ge material 30 is mixed into the underlying SOI film to form an island 50 of substantially SiGe material. Similarly, in this process, for the pFET, the deposited Si:C or optional C material is mixed into the underlying SOI

film forming an island 55 of substantially Si:C material. The thermal annealing process takes place, for example, at about 1200°C to 1350°C between 1 hour and 10 hours, with one implementation at 1200°C for approximately 5 hours.

By using the method of the invention, the required Ge% is not large (e.g., less than 25% and in one implementation 10 to 20%) for the nFET and thus does not cause defect issues. Also, due to the high temperature thermal mixing step, for example, the STI 25 can relax and facilitate the relaxation of the SiGe island 50 and Si:C island 55. This is due, in part, because the STI comprises oxide material, which is a viscous material at the high temperature, e.g., becomes a low viscosity material at high temperature.

Also, it should now be understood that the SiGe island 50 and the Si:C island 55 have different relaxed crystal lattice (different dimensions between the atoms) which yield a unique substrate with small crystal islands. The relaxation of the SiGe island 50 and the Si:C island 55 provides improved performance as compared to blanket (SiGe or Si:C) substrates. In an implementation, high temperature stable amorphous material, e.g., SiO_2, between the SiGe island 50 and the Si:C island 55 and the crystal on insulator structure are thus used in accordance with the invention.

Figures 7-10 show another aspect of the invention. In Figure 7, a silicon wafer such as SOI is shown. As in the previously described structure, the SOI may be fabricated using the SIMOX process or other well known processes. An Si layer 20 is patterned to form shallow trench isolation (STI) 25 using standard techniques of pad oxidation, pad nitride deposition, lithography based patterning, reactive ion etching (RIE)

of the stack consisting of nitride, oxide, and silicon down to the buried oxide, edge oxidation, liner deposition, fill deposition, and chemical mechanical polish. The STI formation process is well known in the art.

Referring to Figure 8, a pFET mask 40 is provided on a portion of the structure at locations of the yet to be formed pFET. The pFET hard mask may be deposited using convention techniques such as chemical vapor deposition methods. For example, such techniques may include spin-on coating, CVD, plasma-assisted CVD, evaporation ultrahigh vacuum chemical vapor deposition (UHVCVD), rapid thermal chemical vapor deposition (RTCVD), limited reaction processing CVD (LRPCVD) and other like deposition processes.

An epitaxial Ge layer 30 is selectively grown over the exposed surface of the yet to be formed nFET using conventional techniques. In one embodiment, the thickness of the Ge material may range from 5 to 50 nanometers, or other dimension depending on the thickness of the underlying Si layer which may, for example, range from 30 to 100 nanometers. The hard mask 45 is stripped using well known processes, as discussed above.

In Figure 9, an nFET mask 35 is provided on a portion of the structure at locations of the yet to be formed nFET. The nFET hard mask may be deposited using conventional techniques such as chemical vapor deposition methods as discussed throughout and which should be known to those of ordinary skill.

An Si:C layer 40 is selectively grown over the exposed surface of the structure at the yet to be formed pFET using conventional techniques such as chemical vapor deposition method, as discussed above. In one embodiment, the thickness of the Si:C material may range from 5 to 50 nanometers, or other dimension depending on the thickness of the underlying Si layer which may, for example, range from 30 to 100 nanometers. The C may even be thinner ranging from 1 to 50 nanometers.

As shown in Figure 10, the nFET hard mask 35 is then removed using well known processes. The structure then undergoes a thermal annealing process. During the annealing process, for the nFET device, the Ge material 30 is mixed into the SOI film forming an island 50 of substantially SiGe material. Similarly, for the pFET, the Si:C or optionally C material is mixed into the SOI film forming an island 55 of substantially Si:C material. This process also forms a BOX layer, as the substrate. The thermal annealing process takes place, for example, at about 1200°C to 1350°C between 1 hour and 10 hours, with one implementation at 1200°C for approximately 5 hours.

As discussed above, and similar to the previous implementations, by using the method of the invention, the required Ge% is not large (e.g., less than 25% and in one implementation from 10 to 20%) and thus does not cause defect issues. Also, due to the high temperature thermal mixing, for example, the STI 25 can relax and facilitate the relaxation of the SiGe island 50 and Si:C island 55. As previously discussed, the relaxation of SiGe and Si:C provides improved performance as compared to blanket (SiGe or Si:C) substrates. In one implementation of the invention, the element of such

structure is the use of high temperature stable amorphous material, e.g., SiO_2, between the islands and the crystal on insulator structure.

In another aspect of the invention, C can be implanted at high dose into the pFET region which can produce concentrations much greater than the 1-4% C in the Si:C upon thermal annealing. The dose may be about 1 e 16 #/cm^2 or greater such as 5 e 16 #/cm^2 .

Now, using either of the intermediate structures of Figure 6 or Figure 10, a tensile hard mask is deposited on the structure as shown in Figure 11. In one implementation, the hard mask is nitride, and is deposited in any known conventional manner over the structure. For example, the nitride hard mask may be hard mask formed using a conventional deposition process such as spin-on coating, CVD, plasma-assisted CVD, ultrahigh vacuum chemical vapor deposition (UHVCVD), rapid thermal chemical vapor deposition (RTCVD), limited reaction processing CVD (LRPCVD) and other like deposition processes. In one implementation, the hard mask is deposited to a range from 5 to 50 nanometers, or other dimension depending on the thickness of the underlying layers.

Thereafter, as shown in Figure 12, a sidewall image transfer and etch is performed in a conventional manner to form the fins 75 and 80. For example, the fins are defined by Sidewall-Image Transfer Lithography, which places fins on the perimeter of drawn rectangles (mandrels). Subsequently a trim mask is used to remove undesired parts of loops and a conventional resist mask is used to block off source and drain regions (not

shown) to link the fins together. During this process, the hard mask 70 remains as a cap of the nFET and pFET regions.

In Figure 13, an Si epi layer 85 is selectively grown on the sidewalls of the nFET and the pFET. The Si epi layer may grow asymmetrically thus possibly inducing buckling in the nFET due to its highly compressive state, as discussed below. However, the highly tensile hard mask will ensure and even prevent such buckling by substantially equalizing the forces acting on the nFET region during the Si growth.

It should be understood that the lattice constant of the Si epi sidewall layer is different than that of the SiGe and the Si:C "islands" or etched fins. For example, in implementation, the SiGe has a lattice constant $a \geq$ aSi and the Si:C has a lattice constant $a \leq$ aSi. That is, standing alone, the Si normally has a lower lattice constant than the SiGe layer; namely, the lattice constant of the Si material does not match the lattice constant of the SiGe layer. However, in the structure of the invention, the lattice structure of the Si sidewall layer will tend to match the lattice structure of the SiGe. Thus, by virtue of the lattice matching of the Si (which normally is smaller) to the SiGe layer, the Si layer is placed under a tensile stress. This area will act as a strained channel for the nFET. In one embodiment, the Ge content of the SiGe layer may be less than 25% in ratio to the Si content.

Also, standing alone, Si would normally have a larger lattice constant than the Si:C. That is, the lattice constant of the Si material does not match the lattice constant of the Si:C. However, in the structure of the invention, the lattice structure of the Si layer

will tend to match the lattice structure of the Si:C . By virtue of the lattice matching of the Si (which normally is larger) to the Si:C island, the Si layer is placed under a compressive stress. That is, similar to the occurrence with the SiGe, the surrounding areas of the Si:C island will try to obtain an equilibrium state thus resulting in a compressive stress of an epitaxial Si sidewall layer formed on the Si:C. This area will act as a strained channel for the pFET. In one embodiment, as deposited, the C content may be up to about 4% in ratio to the Si content.

The structure formed, as shown in Figure 13, is an intermediate structure that accommodates formation of semiconductor devices, such as pFETs and nFETs, in accordance with the principles of the invention. To form the final device, CMOS processes may be performed to form n and p finFET devices on the structure, as is well known in the finFET art. For example, the devices may include ion implantation of source and drain regions separated by the semiconducting channel of strained SiGe and Si:C. That is, the nFET will be formed over the tensilely strained channel and the pFET will be formed over the compressively strained Si channel. A gate dielectric is provided atop the strained channel, and a gate conductor is provided on top of the gate dielectric.

While the invention has been described in terms of embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims. For example, the invention can be readily applicable to bulk substrates.